REMARKS

A set of corrected, formal drawings are submitted with the present amendment, in response to the objection thereto in paragraph 1 of the Office Action. Claims 1-24 remain pending with the present amendments. In the Office Action, all claims were rejected under 24 U.S.C. §103 as being obvious over U.S. Patent No. 4,918,692 to *Hidaka* et al. ("Hidaka"), in view of U.S. Patent No. 5,278,839 to *Matsumoto* et al. ("Matsumoto"), and further in view of U.S. Patent No. 5,748,543 to *Lee* et al. ("Lee"), or further in view of other cited references as indicated in the Office Action. For the reasons set forth below, Applicants respectfully submit that the claims as amended herein are distinguished from the references cited by the Examiner. Reconsideration and withdrawal of the rejections is respectfully requested.

As amended herein, claim 1 recites an ECC-based method for self-repair of a failed memory element within an integrated circuit. In such method, the locations of memory failures within an integrated circuit are automatically identified and recorded by processing data and check bits retrieved from addressed memory locations, the processing being performed within the integrated circuit. First logic circuits within the integrated circuit are used to automatically identify failure patterns based on the recorded locations. In addition, at least second logic circuits are used within the integrated circuit to automatically replace a failed memory element within the integrated circuit with a redundancy element based on at least one of the identified failure patterns.

Clearly, claim 1 is neither taught nor suggested by the combination of references

used by the Examiner to reject the claims. *Hidaka* merely describes an integrated circuit in which an error correction code is used to detect and correct errors in stored data, but which has no ability to identify and record the locations of memory failures within the integrated circuit. *Hidaka* neither teaches nor suggests processing, within the integrated circuit, data bits and check bits retrieved from addressed memory locations to identify and record the locations of memory failures within the integrated circuit. Rather, Hidaka merely describes the well-known practice of identifying the locations of failed memory bits by placing the integrated circuit in an external test fixture (FIG. 12) having an external tester 31, to determine the locations of such failures. (col. 10, lns. 10-11).

Neither does *Matsumoto* or *Lee* provide the teachings which *Hidaka* lacks with respect to the presently claimed invention. *Matsumoto* merely describes a system capable of self-check and self-repair but which clearly does not identify and record locations of memory failures within an integrated circuit by processing, performed within the integrated circuit, of data bits and check bits retrieved from addressed memory locations of the integrated circuit. Rather, *Matsumoto* only describes a chip which, rather than retrieving data bits and check bits from addressed memory locations, identifies the locations of defects by writing test data to a memory of the chip, retrieving, i.e., reading, the previously written test data back from the memory, and then comparing the test data that is read back from the memory with the original test data that was written.

Neither does *Lee* teach or suggest identifying and recording the locations of memory failures by processing data bits and check bits retrieved from addressed memory locations of the memory. The passage in *Lee* cited by the Examiner at col. 3,

lns. 31-36 merely describes a circuit which selects a spare column instead of the default column of the memory when a defect signal indicates a defect in at least two normal memory cells in different rows and the same column of the memory.

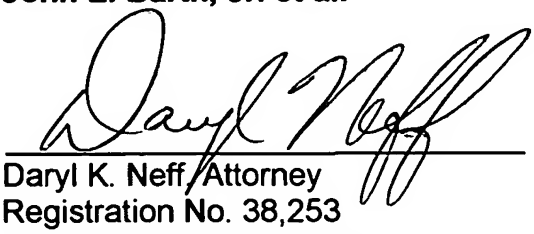
Clearly none of the references either teaches or suggests identifying locations of memory failures within an integrated circuit by processing data bits and check bits, recording the locations, identifying failure patterns based on the recorded locations, and replacing a failed memory element based on the failure pattern identified in such manner. Moreover, there is no motivation provided from the references to combine them in the manner such as asserted by the Examiner to result in the claimed invention. Only by hindsight, gleaned from knowledge of Applicants' invention itself, might the asserted combination be made.

The remaining references merely describe certain circuits and methods which are not related to the fundamental method and apparatus for self-repair of a failed memory element recited in the presently amended claims. Accordingly, Applicants submit that the present claims are fully distinguished over the references cited by the Examiner. Reconsideration and withdrawal of the rejections are respectfully requested.

If for any reason the Examiner has any question regarding the content of this amendment or the allowability of the presently pending claims, he is respectfully requested to contact the Applicants' undersigned attorney at the telephone number indicated below.

This Amendment is submitted together with a petition under 37 CFR 1.136(a) for a one-month extension of time. Otherwise, it is believed that no other fee is required upon filing this Amendment. However, if any fee is required, authorization is given to debit the Deposit Account No. 09-0458 of the Assignee for the amount due, and to credit any overpayment to the same account.

Respectfully submitted,
John E. Barth, Jr. et al.

By: 

Daryl K. Neff, Attorney
Registration No. 38,253
Telephone: (973) 316-2612